



(Use as many sheets as necessary)

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Application Number	10/730,388
Filing Date	December 07, 2003
First Named Inventor	Buxton, et al.
Art Unit	2863
Examiner Name	Khuu, Cindy D.
Attorney Docket Number	TAI.0800

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

**Examiner
Signature**

Gindy Khum

Date
Considered

12-11-06

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		<i>Complete if Known</i>	
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Sheet 2 of 5	Attorney Docket Number		TAI.0800

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CKH		SINGH Et al., Screening for Known Good Die (KGD) Based on Defect Clustering: An Experimental Study, IEEE	
		SINGH, Position Statement: Good Die in Bad Neighborhoods, IEEE	
		MILLER, Position Statement: Good Die in Bad Neighborhoods, IEEE	
		ROEHR, Position Statement: Good Die in Bad Neighborhoods, IEEE	
		MANN, "Leading Edge" of Wafer Level Testing	
		MICHELSON, Statistically Calculating Reject Limits at Parametric Test, IEEE	
		SABADE et al., Immediate Neighbor Difference IDDQ Test (INDIT) for Outlier Detection, Dept. of Computer Science – Texas A&M University	
		HUANG, et al., Image Processing Techniques for Wafer Defect Cluster Identification, IEEE	
		SABADE, et al., Use of Multiple IDDQ Test Metrics for Outlier Identification, Dept. of Computer Science – Texas A&M University	
CKH		CHEN, et al., A Neural-Network Approach to Recognize Defect Spatial Pattern in Semiconductor Fabrication, IEEE	

Examiner Signature	Cindy Khuu	Date Considered	12-11-06
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CML		SAPOZHNIKOVA, et al., The Use of dARTMAP and FUZZY ARTMAP to Solve the Quality Testing Task in Semiconductor Industry, IEEE	
		SIKKA, Automated Feature Detection & Characterization in Sort Wafer Maps,	
		HANSEN, et al., Process Improvement Through the Analysis of Spatially Clustered Defects on Wafer Maps	
		DENBY, et al., A Graphical User Interface for Spatial Data Analysis in Integrated Circuit Manufacturing, AT&T Bell Laboratories	
		FRIEDMAN, et al., Model-Free Estimation of Defect Clustering in Integrated Circuit Fabrication	
		HANSEN, et al., Monitoring Wafer Map Data From Integrated Circuit Fabrication Processes for Spatially Clustered Defects	
		XU, Statistical Problems in Semiconductor Manufacturing	
		THOMAS GNIETING, Measurement Related and Model Parameter Related Statistics	
✓		Agilent PDQ-WLR(tm) Test and Analysis Software Environment - Product Note, Agilent Technologies, 2000	
CML		Advance Parametric Tester with HP SPECS, Hewlett-Packard Company, 1999	

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CML		JEFF CHAPPELL, LSI Applies Statistics to Defectivity, 4/14/2003 (http://www.reed-electronics.com/electronicnews/index.asp?layout=articlePrint&articleID=CA292185)	
		ERIK JAN MARINISSEN, et al., Creating Value Through Test, IEEE 2003, 1530-1591	
		RUSSELL B. MILLER, et al., Unit Level Predicted Yield: a Method of Identifying High Defect Density Die at Wafer Sort, IEEE 2001, 1118-1127	
		PHILIPPE LEJEUNE, et al., Optimizing Yield vs. DPPM for Parts Average Testing, www.galaxysemi.com	
		EMILIO MIGUELANEZ, et al., Advanced Automatic Parametric Outlier Detection Technologies for the Production Environment,	
		Guidelines for Part Average Testing, Automotive Electronics Council, AEC-Q001-Rev-C July 18, 2003	
		ZINKE, KEVIN, et al. Yield Enhancement Techniques Using Neural Network Pattern Detection, IEEE 1997, 211-215	
		LEJEUNE, PHILIPPE et al., Minimizing Yield Loss with Parts Average Testing (PAT) and Other DPM Reduction Techniques, Tetradyne Users Group, 2006	
CBL		LEJEUNE, PHILIPPE et al., Minimizing Yield Loss with Parts Average Testing (PAT) and Other DPM Reduction Techniques (PRESENTATION), Tetradyne Users Group, 2006	

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CHU		Defecter(tm)II - Defect Data Analysis Software, Semicon	
		STANLEY, JAMES, Spatial Outlier Methods for Detecting Defects in Semiconductor Devices at Electrical Probe, Motorola	
		RATCLIFFE, JEFF, Setting a Nearest Neighbor IDDQ Threshold,	
		DAASCH, ROBERT, Variance Reduction Using Wafer Patterns in Iddq Data, Proceeding of International Test Conference October 2000, pp 189-198	
CHU		DAASCH, ROBERT, Neighbor Selection for Variance Reduction in Iddq and Other Parametric Data, ITC International Test Conference, IEEE 2001	

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